Advanced High Speed Design

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Agenda

1. Signal Integrity in High Speed PCBs
2. Channel Characterization
3. Analysis of Transmission Line Styles

Signal Integrity Challenges in High Speed PCBs

Why Focus on SI/PI/EMI?

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- Most of what you do in high speed PCB design is intended to ensure signal integrity (SI).
- **Related:** Power integrity
- **Related:** Electromagnetic interference
- Determined by a few critical areas:
  - Stackup/material selection
  - Differential interconnect design and routing
  - Stable power system design
  - Noise coupling between interconnects

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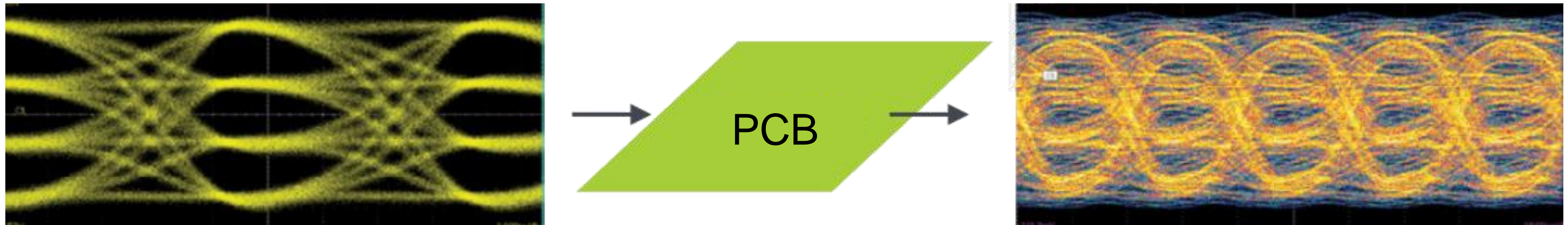
- Signals → Analyzed in the time domain
- Channels → Analyzed in the time or frequency domain
- Metrics: S-parameters, impedance, inter-symbol interference (ISI), jitter, channel operating margin (COM),…



PAM4 Signaling in High-Speed Serial Technology: Test, Analysis, and Debug. Tektronix Application Note, July 2018.

Example with 56G channels on Eurocard backplane (6U)

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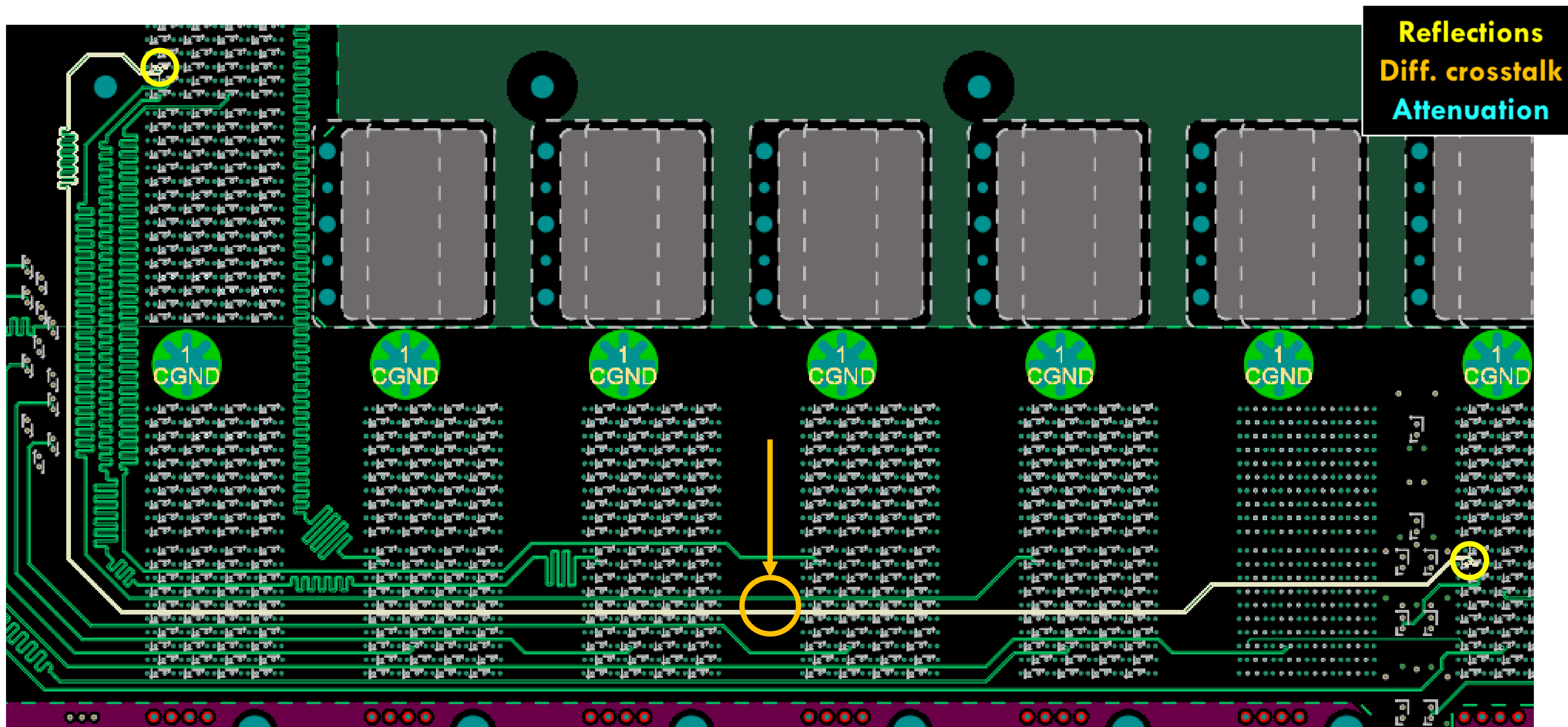

Digital Signals and Rise Time

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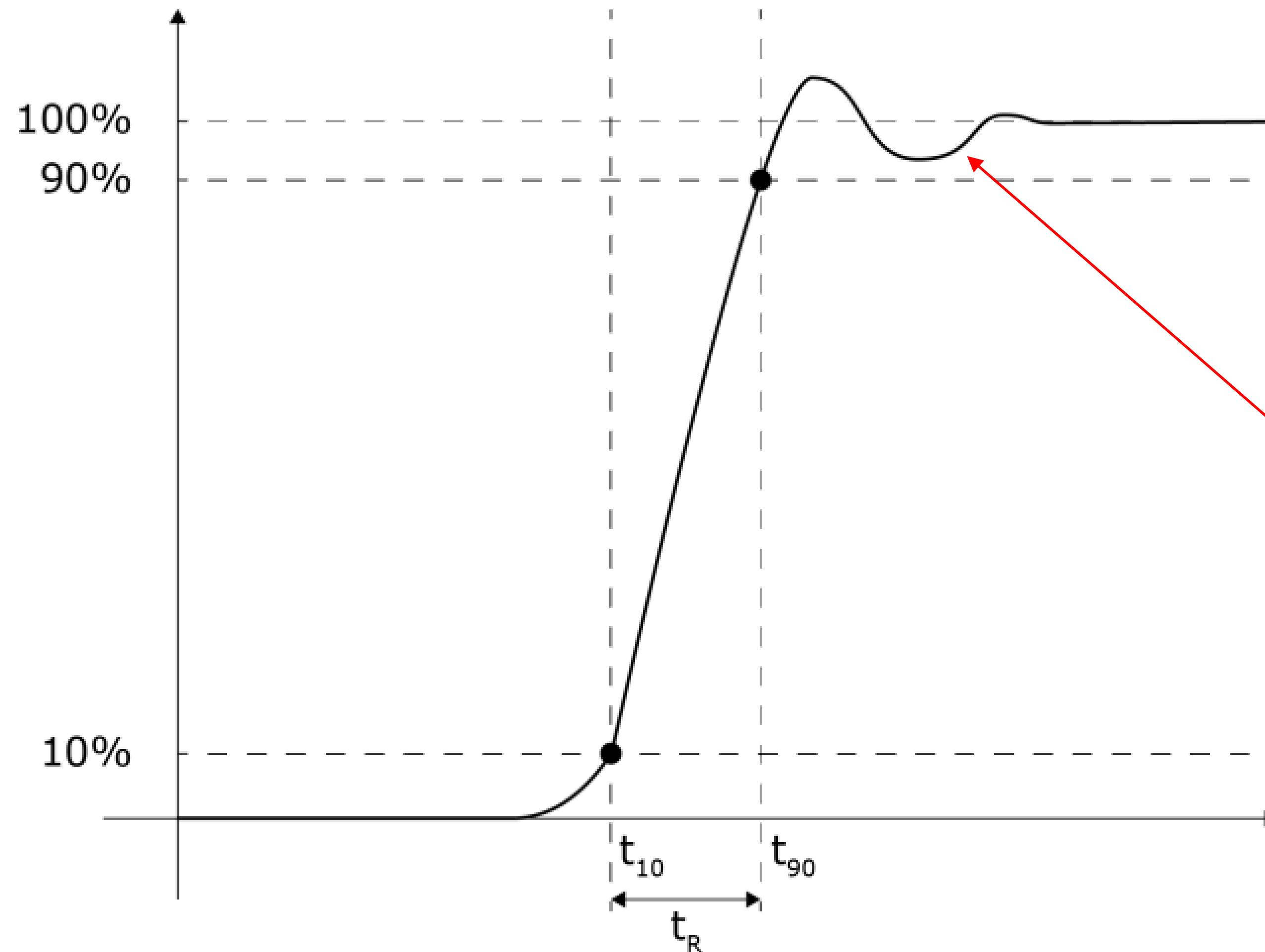
- Signal rise time ($\frac{dI}{dt}$ and $\frac{dV}{dt}$) governs electrical behavior



- Crosstalk
- Radiated emissions
- Measurement artifacts (Gibbs)
- Transient phenomena
- Resonant phenomena

Loss Mechanisms

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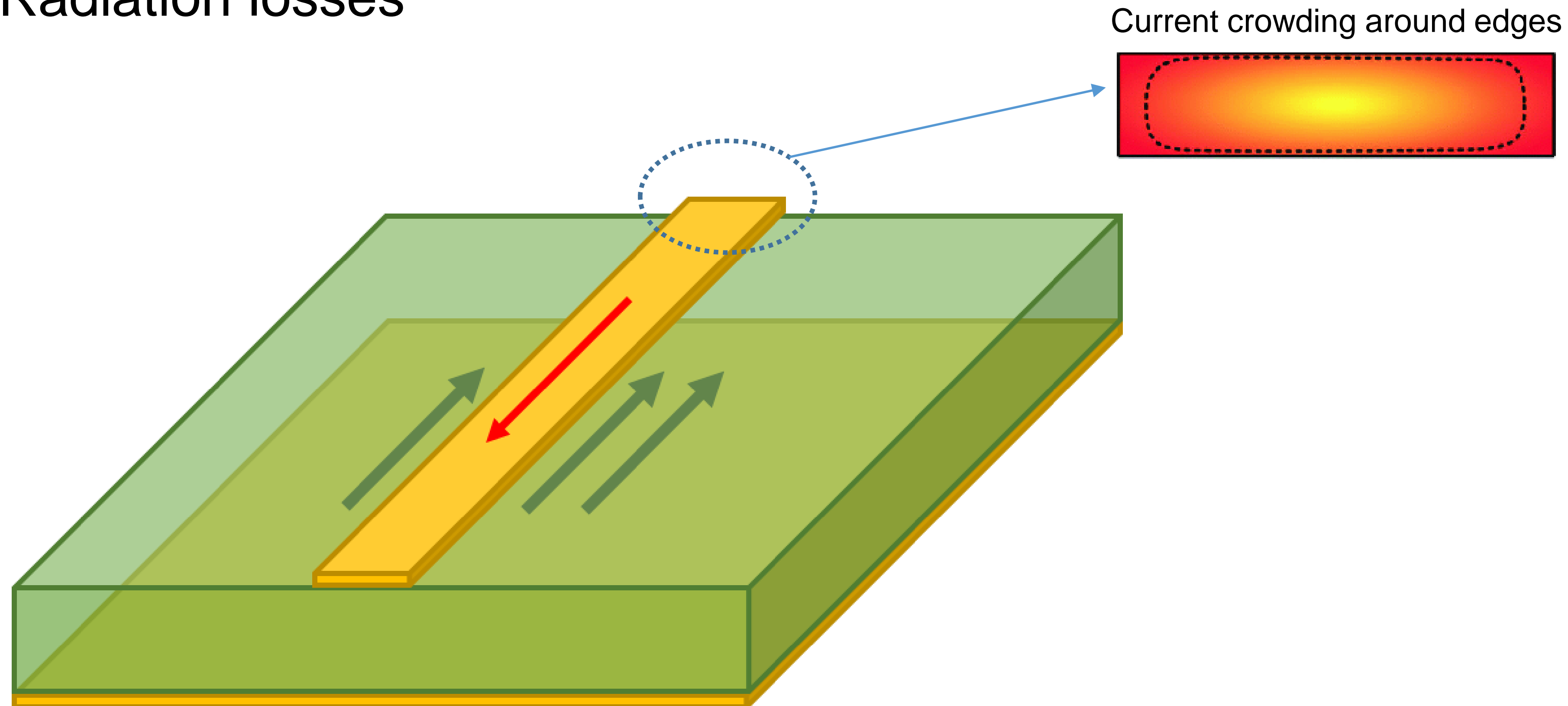
- Dielectric losses
- Copper losses (DC, skin effect, roughness)
- Plating and solder mask create additional losses
- Radiation losses



Real Signal Integrity Metrics

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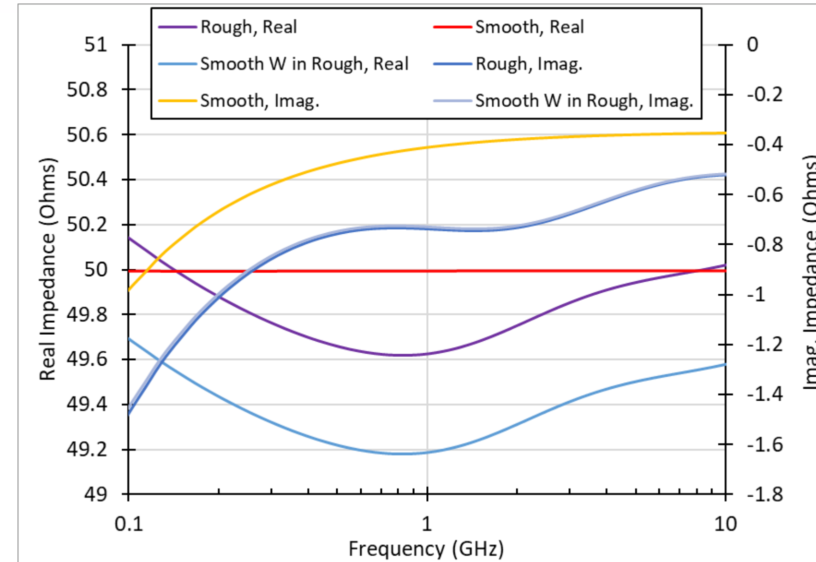
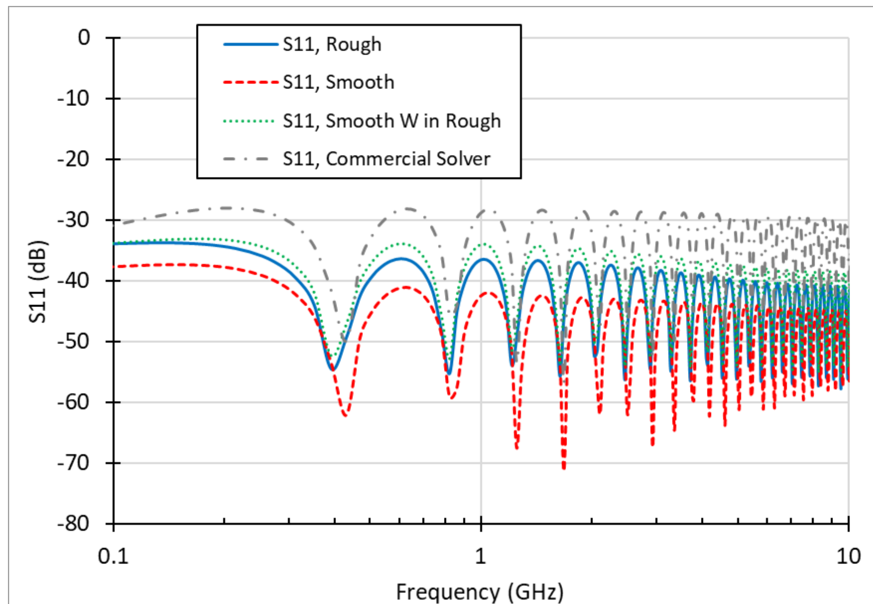
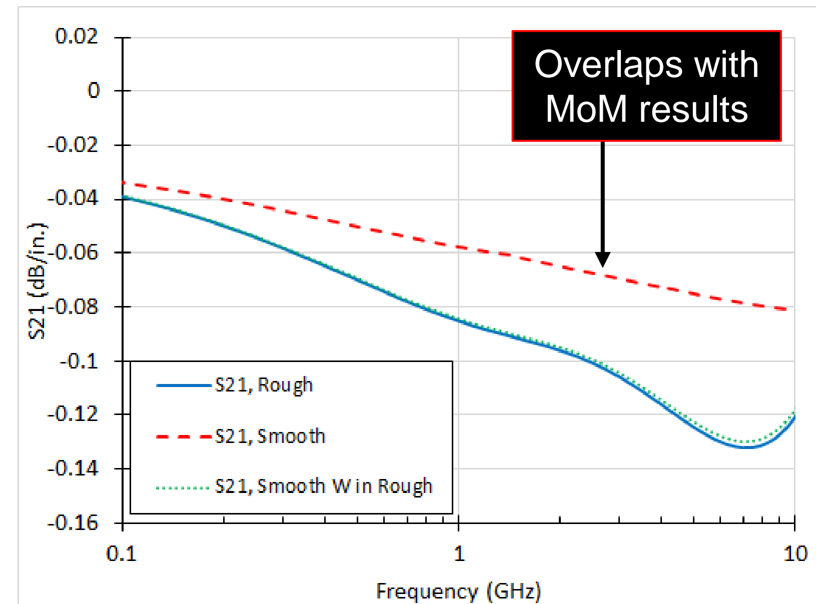
- **Rough line:** W = 0.178 mm (6.996 mil)
- **50 Ω Smooth line:** W = 0.180 mm (7.085 mil) → No dispersion or skin effect
- **Smooth dispersion-less line:** $\varepsilon = 4.171 + 0.0576i$ (@ 1 GHz)
- Commercial MoM solver says 49.99 Ohms at 7.614 mils







Inhomogeneities Lead to Skew

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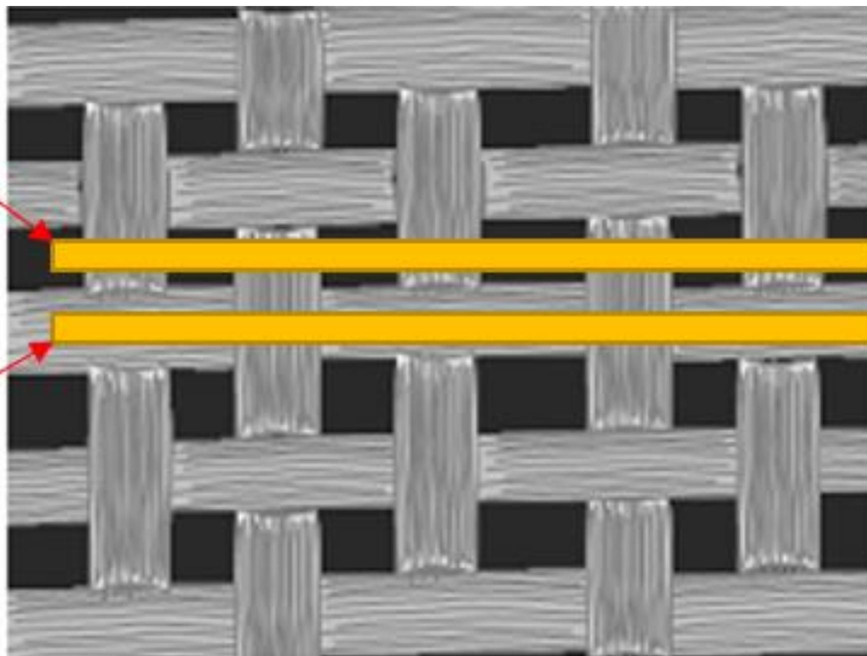
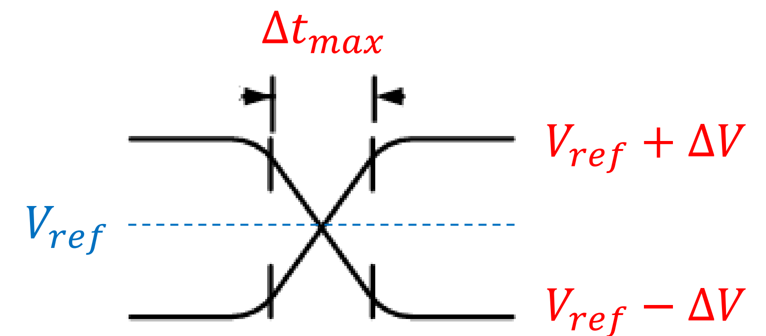
- Signal rise time can be used to find a very large length matching tolerance (sometimes this will be several cm)

- **However:** this assumes perfect channels!

$\varepsilon_{resin} < \varepsilon_{fiber}$



Still skew with perfect length matching!



What are the other sources of skew/jitter?

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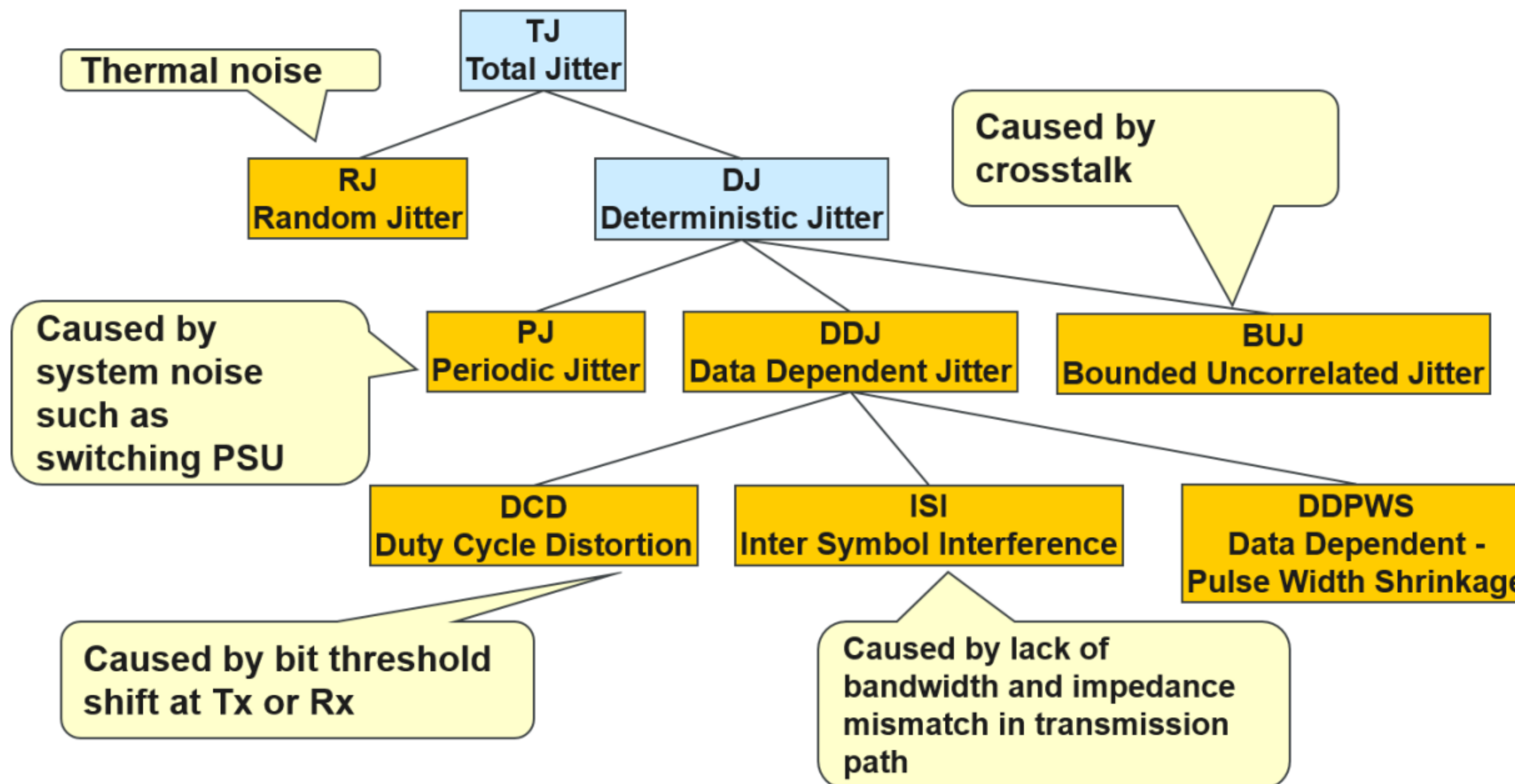
- Jitter is best defined as “the sum of all skews” (Steve Corrigan, Texas Instruments)



Anritsu. *A Guide to Making RF Measurements for Signal Integrity Applications*. 2016.

Channel Characterization

Objectives in Channel Characterization

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- Determine magnitude of SI problems
- Find potential cause of SI problems
- Determine course of action to eliminate the problem
- **Example:** Layer thickness and routing – should these be changed?
- **Example:** Prepreg vs. core order

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Analytical

- Numerical methods:
  - 2D field solvers w/BEM or MoM
  - 3D field solvers
  - SPICE
  - IBIS
- By hand with formulas or mixed formulas/tabulated data
- Dispersive losses → **requires wideband analysis**

Experimental

- Oscilloscope w/ eye diagram
- VNA (S-parameter measurements)
- Spectrum analyzer + arbitrary waveform generation
- **Probe and instrument characteristics must be known**

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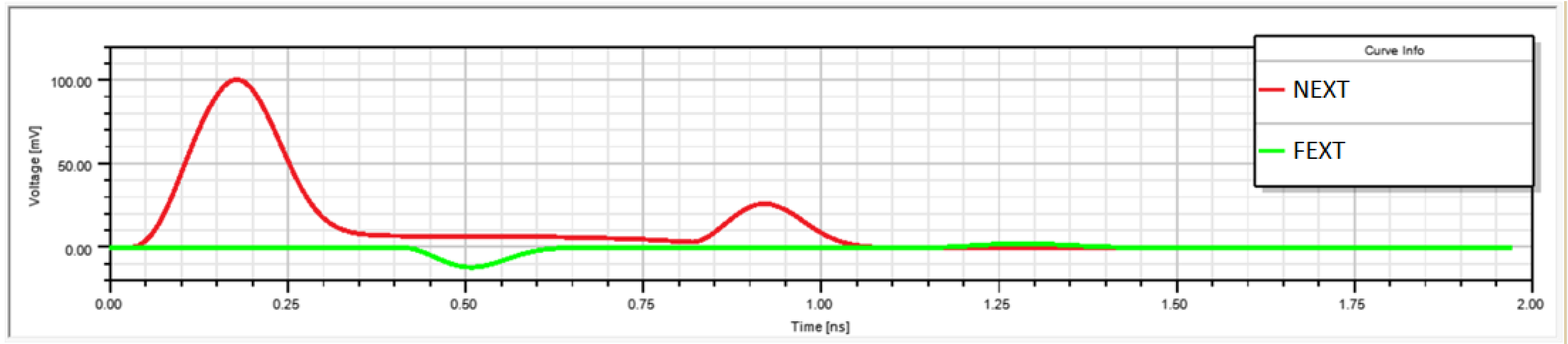
- Near-end and far-end crosstalk (NEXT and FEXT)

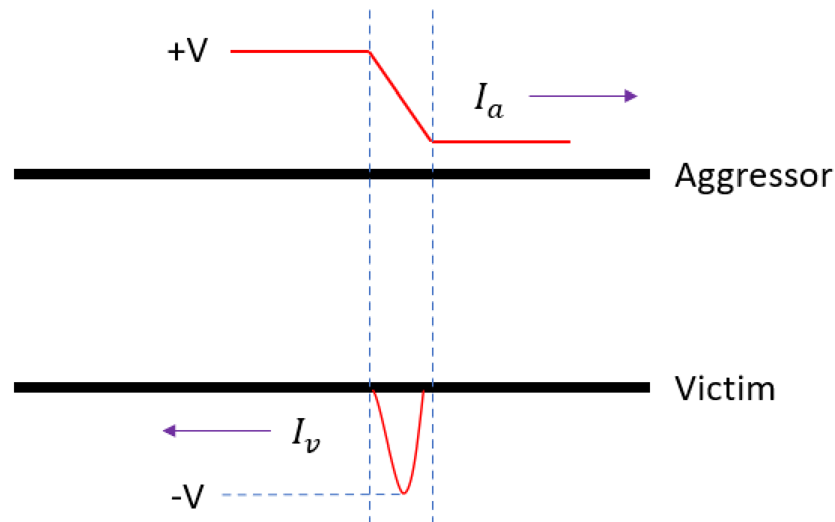


Inductive:

$$V_c = -L_M \frac{dI_A}{dt},\ I_c = \frac{V_c}{Z_0}$$

Capacitive:

$$I_c = C_M \frac{dV_A}{dt},\ V_c = I_c Z_0$$

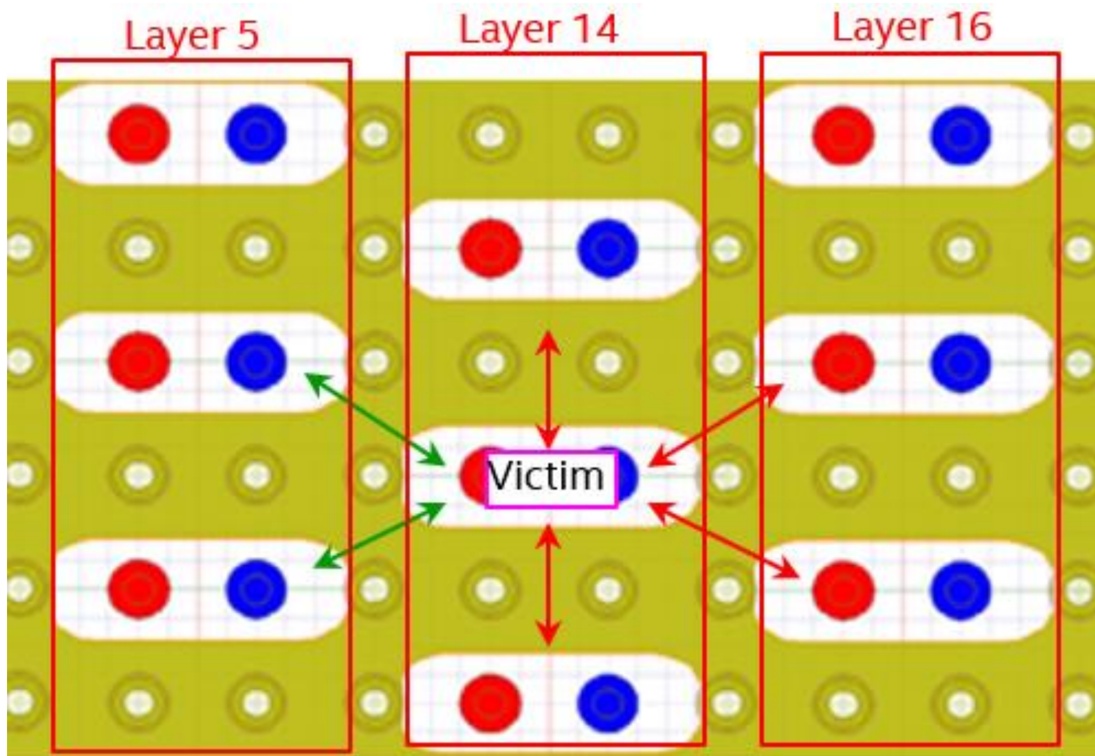


$$NEXT = \frac{1}{4} \cdot \left(\frac{length}{vel \cdot t_{rise}} \right) \cdot \left(\frac{C_M}{C_L} + \frac{L_M}{L_L} \right)$$

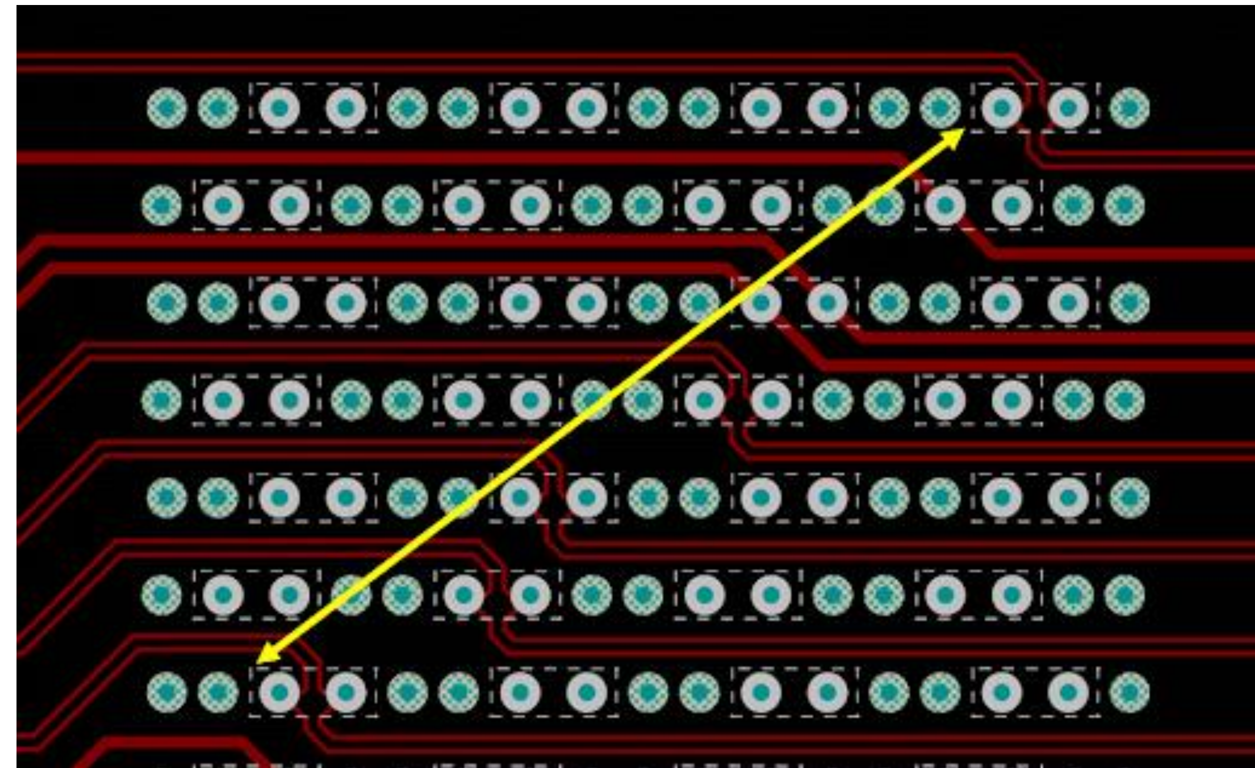
Always ≤ 1

$$FEXT = \frac{1}{2} \cdot \left(\frac{length}{vel \cdot t_{rise}} \right) \cdot \left(\frac{C_M}{C_L} - \frac{L_M}{L_L} \right)$$

- Differential pairs can exhibit crosstalk between each other
- For FPGAs: Plan to stagger vias (same strategy used in OpenVPX backplanes), interleave ground vias



Breakout on FPGA



Bus routing on backplane

Time-domain Reflection Simulation

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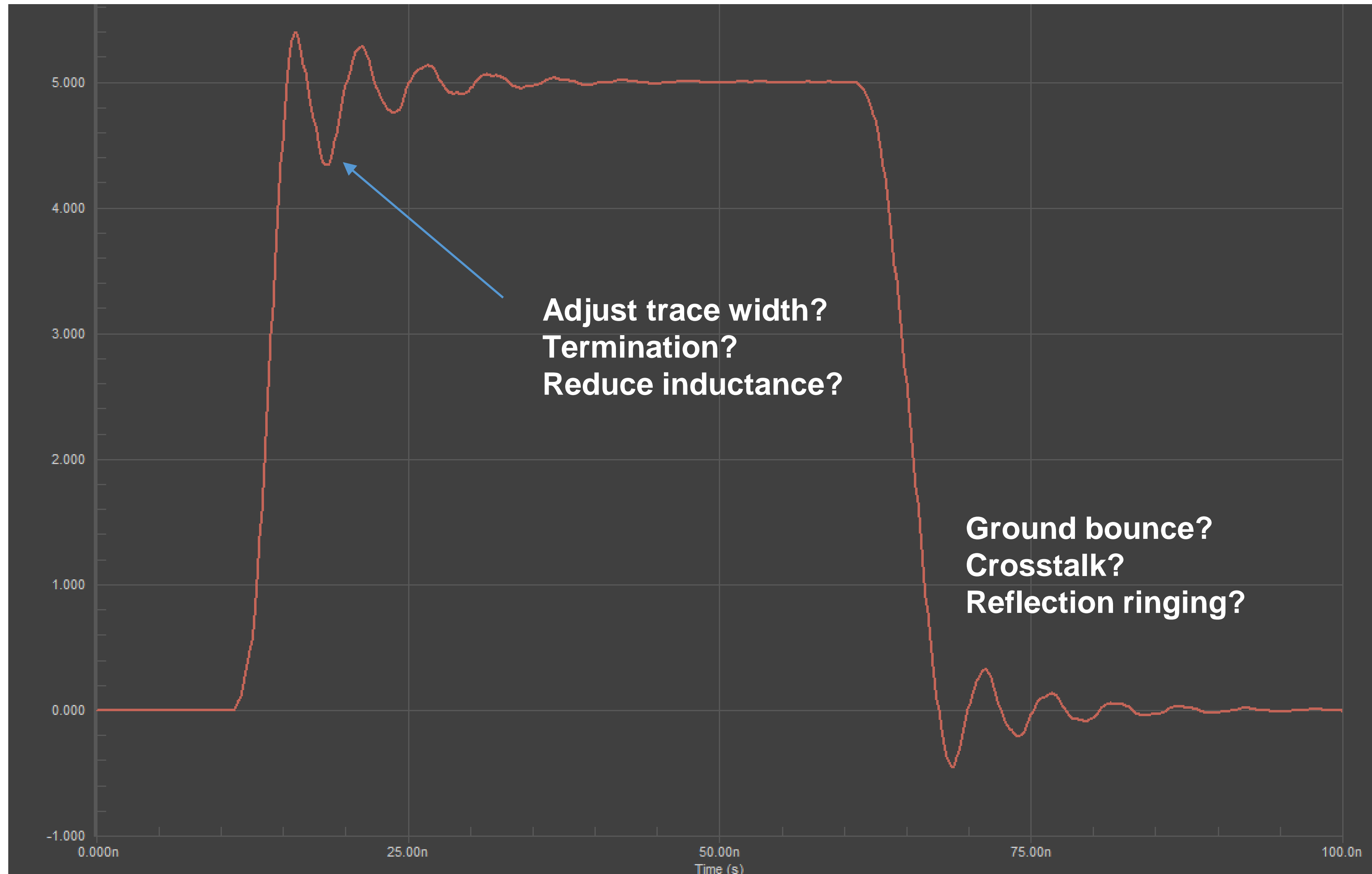
- Can be calculated with same 2D solver as in crosstalk simulations



Eye Diagrams

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- Identify noise and jitter → estimate BER and SNR

Jitter

Noise

Noise Margin

RX Threshold

Eye Diagram

Curve Info

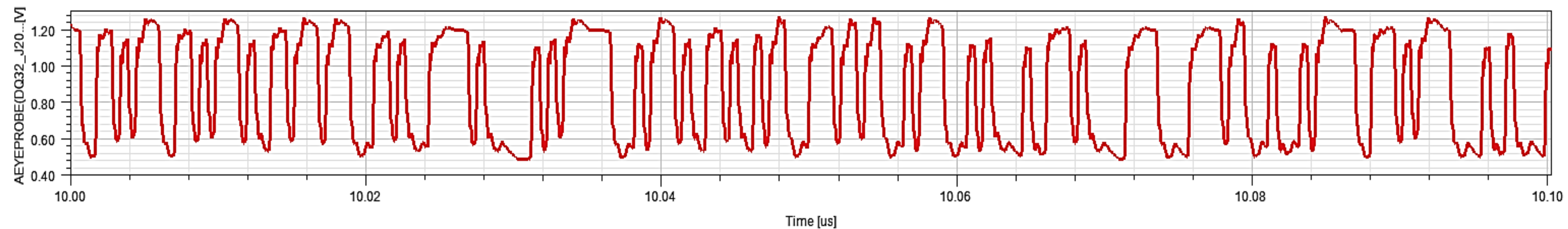
AEYEPROBE(DQ32_J20)

QuickEyeAnalysis

AEYEPROBE(DQ32_J20) [V]

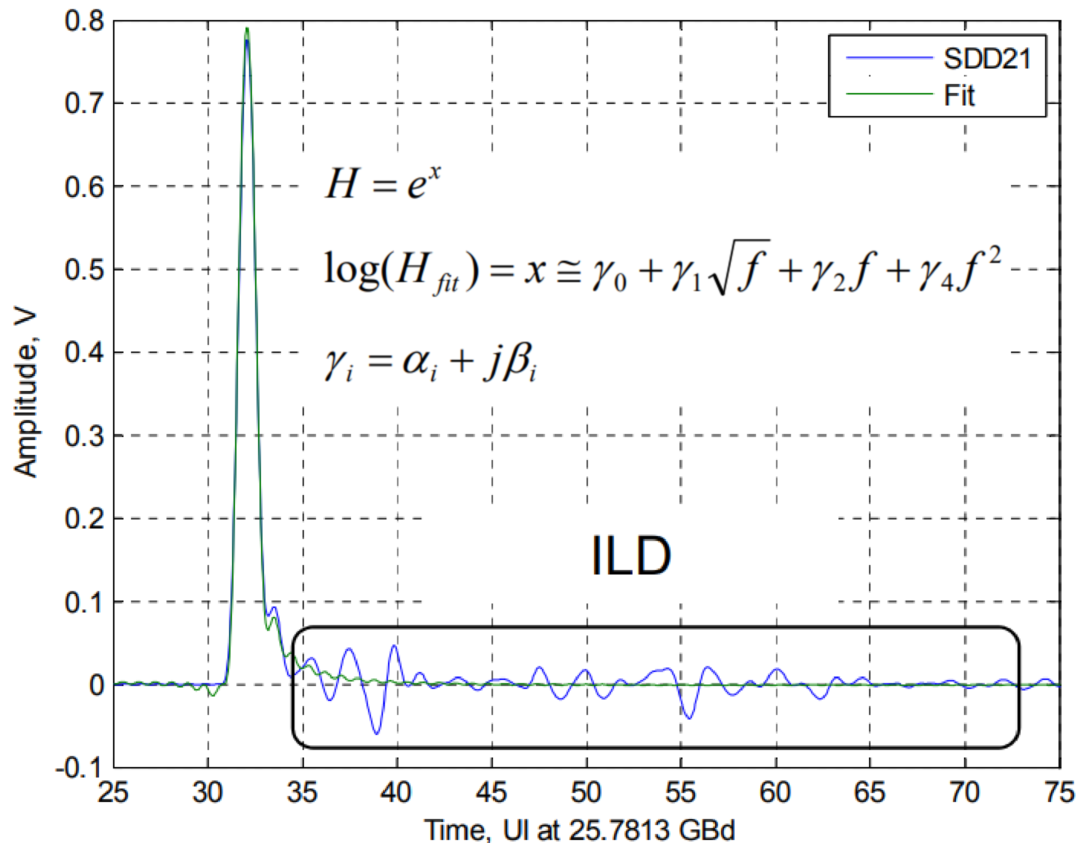
Time [ns]

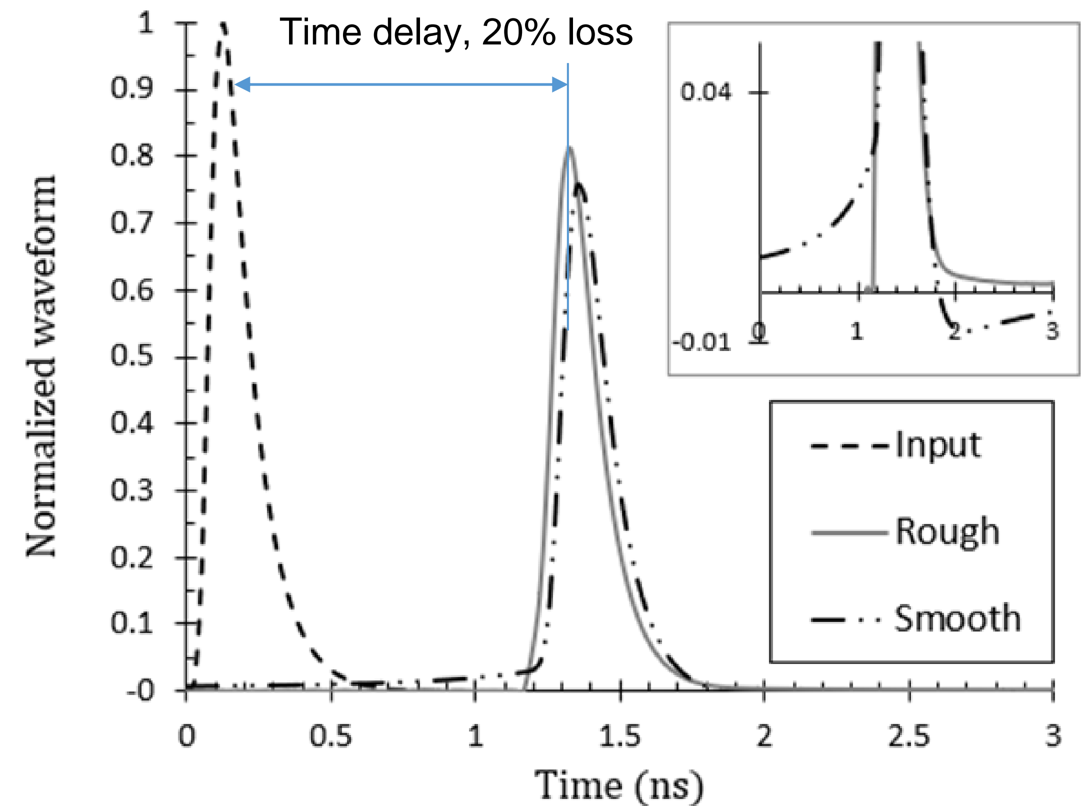
PRBS



More Advanced → Impulse Response

- Identify non-causal effects in channel models
- Identify reflections on the tail-end of impulse response

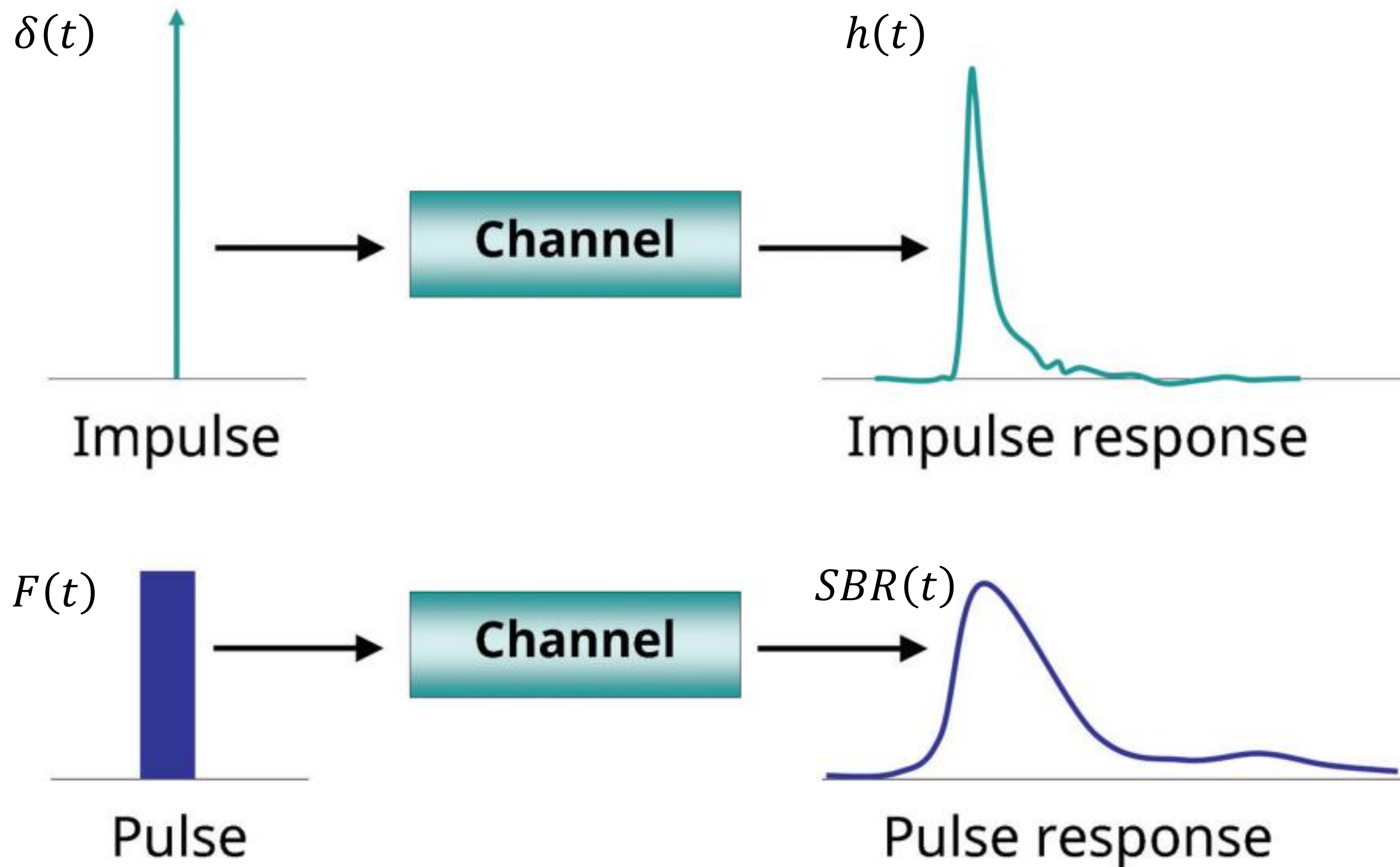




Moore, C., and Healey, A. "A method for evaluating channels." *100 Gb/s Backplane and Copper Study Group*, IEEE, 2011.
Peterson, Z. "Causal Transmission Line Geometry Optimization for Impedance Control in PCBs." *Proceedings of the IEEE Electronics Packaging Society*, 2020.

Single-bit Response From Impulse Response

- Based on channel simulation: determine impulse response, use to calculate single-bit response (SBR)



$$SBR(t) = \int_{-\infty}^{\infty} F(t')h(t-t')dt'$$

Anritsu. *A Guide to Making RF Measurements for Signal Integrity Applications*. 2016.

IBIS (Input/output Buffer Information Specification) Models

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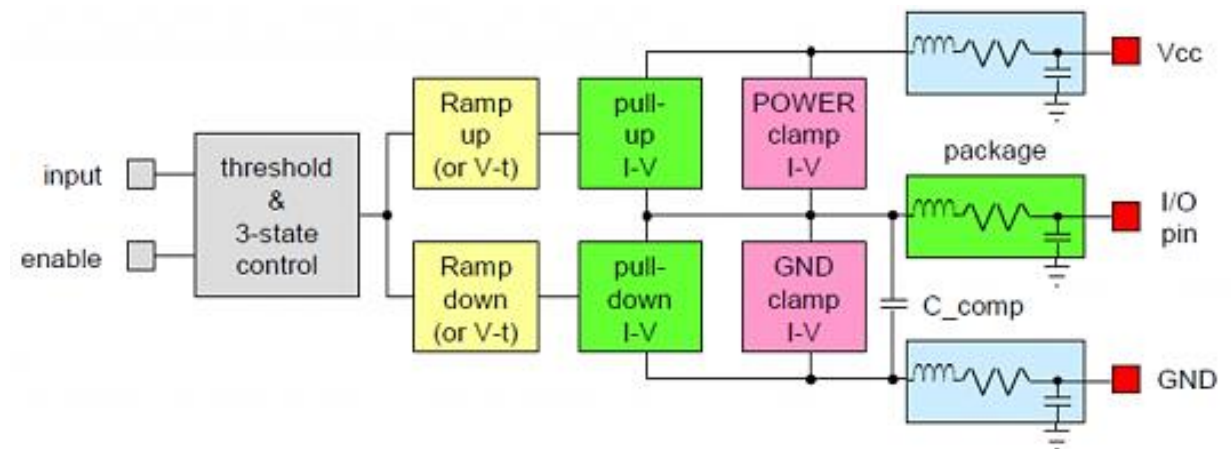
- Behavioral model, faster than SPICE
- Assign model behavior by pin
- Available from manufacturers

Pin Models

Model Name	Model Type
RDY	OPEN_SINK
DQ0	IO
ACC	INPUT
RSTB	INPUT
WEB	INPUT
OEB	INPUT

Model Type: Typical Case

- Models signal behavior on the output buffer in a logic circuit



SPISim. *IBIS model: What is IBIS?* 2015. Source: http://www.spisim.com/blog/ibis-model-what-is-ibis/

Analysis of Transmission Line Styles

Impedance and Propagation

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$$Z_0 = \sqrt{\frac{R+i\omega L}{G+i\omega C}},\ \gamma = \sqrt{(R+i\omega L)(G+i\omega C)} \rightarrow v = \frac{1}{\sqrt{LC}}\ \text{(lossless)}$$

Coplanar microstrip

Coplanar microstrip w/ ground

$$v = \frac{c}{\sqrt{\varepsilon_{R,eff}}}$$

- Lower losses, copper pour allows for thinner 50 Ohm traces

Microstrip

$$v = \frac{c}{\sqrt{\varepsilon_{R,eff}}}$$

- Lower losses, wider traces

Symmetric stripline

Asymmetric stripline

$$v = \frac{c}{\sqrt{\varepsilon_R}}$$

- Higher losses, but traces can be much thinner than on the surface layer

You Could Do It By Hand...

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- Transmission lines: $Z_0 = \sqrt{\frac{R+i\omega L}{G+i\omega C}}$, $\gamma = \sqrt{(R + i\omega L)(G + i\omega C)}$

Incomplete

$$R(\omega) = R_{DC} + \sqrt{\omega} R_s \qquad L(\omega) = L_\infty + R_s / \sqrt{\omega}$$

$$G(\omega) = \omega C(\omega) \tan\delta(\omega) \qquad C(\omega) = K_g \varepsilon_R(\omega) \varepsilon_0$$

- Dielectric constant: $\varepsilon = \varepsilon_R(\omega) + i\varepsilon_I(\omega)$, $tan\delta = \frac{-\omega\varepsilon_I(\omega) - \sigma_{sub}}{\omega\varepsilon_R}$
- Need causal models or data for:

Dielectric constant: $\varepsilon(\omega)$

Copper roughness: $K(\omega)$

Electrical parameters: $R(\omega), L(\omega)$

Zhang, J., et al. "Causal RLGC(*f*) Models for Transmission Lines From Measured *S*-Parameters," *IEEE Transactions on Electromagnetic Compatibility*, 52(1), pp.189-198 (2009).

Transmission Line Transfer Function

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- General definition: $H(f) = \frac{V_L}{V_S} = \frac{Z_L}{AZ_L + B + CZ_SZ_L + DZ_S}$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma l) & Z_0 \sinh(\gamma l) \\ \frac{\sinh(\gamma l)}{Z_0} & \cosh(\gamma l) \end{bmatrix}$$

- Three cases that can be derived by hand from ABCD parameters:

$Z_S = 0$, load terminated with Z_T: $H(s) = \frac{1}{\cosh \gamma l (1 + Z_0 \left(\frac{1 + sZ_TC_L}{Z_T}\right) \tanh \gamma l)}$

$Z_S = Z_0$, load terminated with Z_T: $H(s) = \frac{e^{-\gamma l}}{1 + Z_0 \left(\frac{1 + sZ_TC_L}{Z_T}\right)}$

Unterminated $Z_S = 0$, $Z_L = \frac{1}{sC_L}$: $H(s) = \frac{1}{\cosh \gamma l (1 + Z_0 sC_L \tanh \gamma l)}$

- Approximate the square root: $\gamma = \sqrt{(R + i\omega L)(G + i\omega C)}$

- Take the real part of the result and break into conductor + dielectric

$$\alpha_{total} = \alpha_{conductor} + \alpha_{dielectric}$$

$$\alpha_{dielectric} = 4.34(\omega C Z_0 \tan\delta) \text{ in dB/length}$$

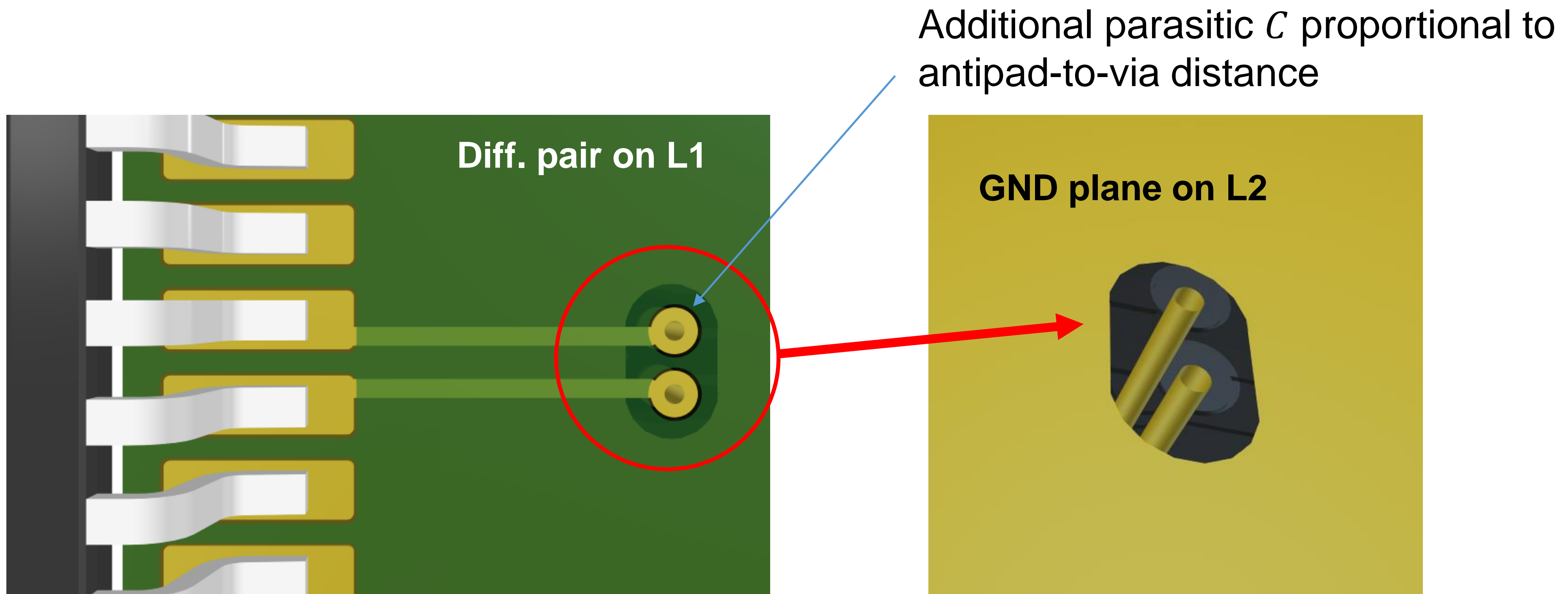
$$\alpha_{conductor} = 4.34\left(\frac{R_{DC} + \sqrt{\omega} K(\omega) R_s}{Z_0}\right) \text{ in dB/length,}$$

4.12 mil dielectric thickness,
unmodified Dk = 4.17/Df = 0.014

	$\alpha_{dielectric}$	$\alpha_{conductor}$ (smooth)	$\alpha_{conductor}$ (rough, Hammerstad)	$\alpha_{conductor}$ (rough, Cannonball-Huray, $a = 2\ \mu m, H = 5\ \mu m$)
Microstrip, 1 GHz	~0.059 dB/inch	~0.053 dB/inch	~0.080 dB/inch	~0.077 dB/inch
Microstrip, 10 GHz	~0.585 dB/inch	~0.14 dB/inch	~0.22 dB/inch	~0.25 dB/inch
Stripline, 1 GHz	~0.067 dB/inch	~0.13 dB/inch	~0.21 dB/inch	~0.19 dB/inch
Stripline, 10 GHz	~0.677 dB/inch	~0.35 dB/inch	~0.53 dB/inch	~0.63 dB/inch

- Antipad shape and size creates parasitic capacitance
- Place with stitching vias to control parasitics

Additional parasitic C proportional to antipad-to-via distance



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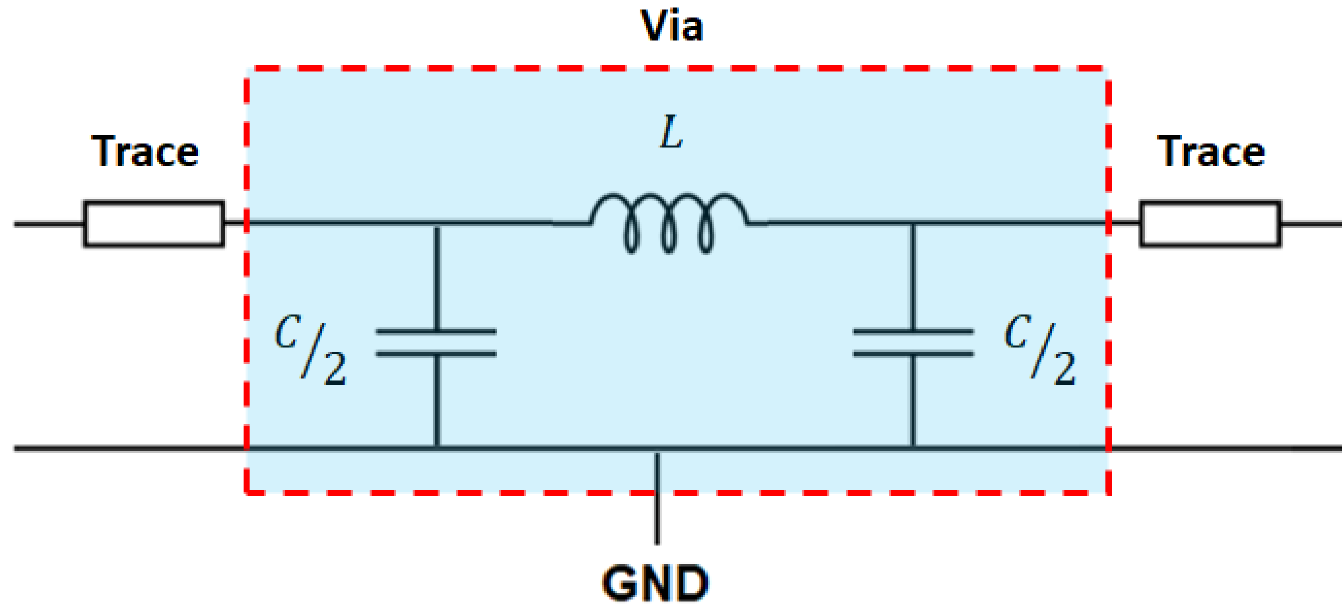
- A simple model for vias and antipads



$$f_{3dB} = \frac{1}{\sqrt{LC}}$$

D_1 = pad diameter
D_2 = antipad diameter
l = via length
d = via barrel diameter

$$L_{via} \approx 5.08l\left(\ln\left(\frac{4l}{d}\right) + 1\right)$$

$$C_{via} \approx \varepsilon_R\sqrt{2}\left(\frac{D_1 l}{D_2 - D_1}\right)$$

Differential Pair Routing and Mode Conversion

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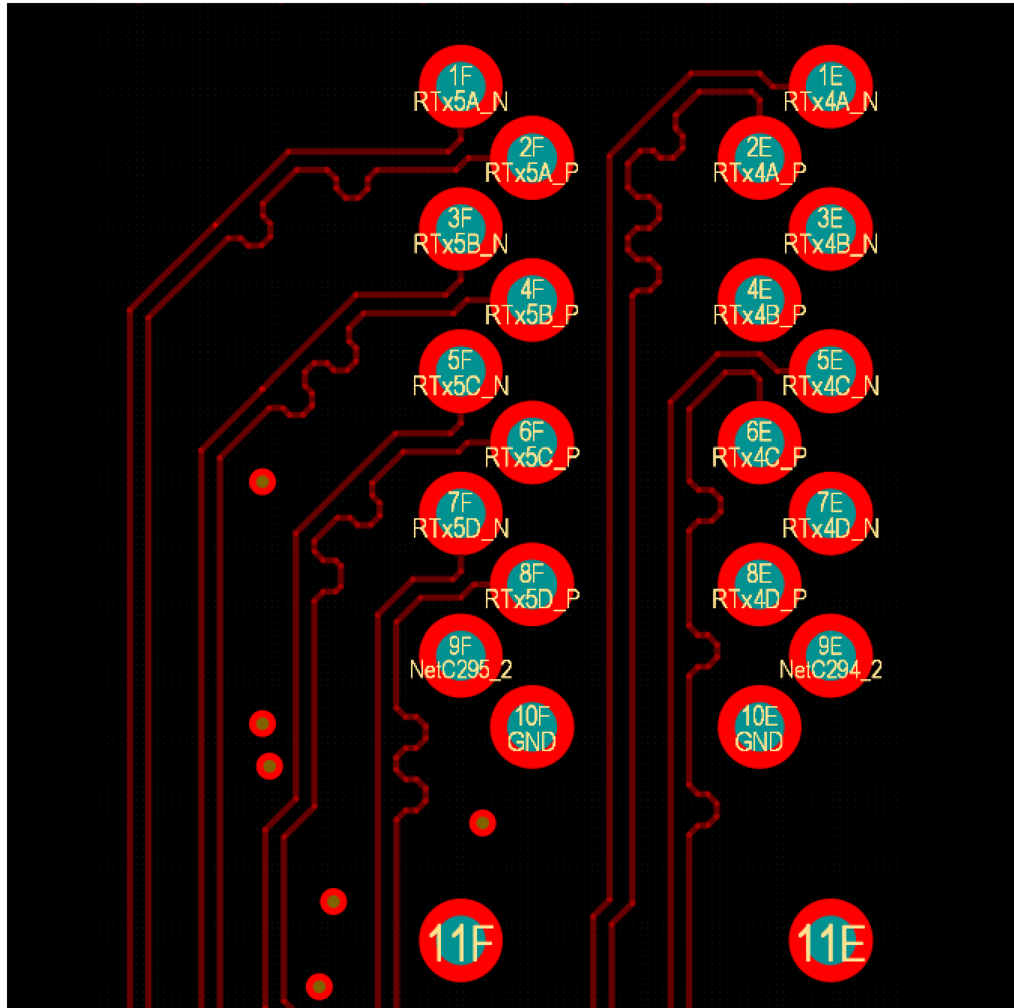
- Add length matching sections near inhomogeneity if possible



Frequency	FCC Class A	FCC Class B
<1.7 MHz*	40 uA	10 uA
1.7 - 30 MHz*	120 uA	10 uA
30 MHz**	24 uA	8 uA
50 MHz**	14 uA	5 uA
100 MHz**	11 uA	3.5 uA

** Based on Conducted Emission Limits*

*** Based on Radiated Emission Limits*

Via Stubs

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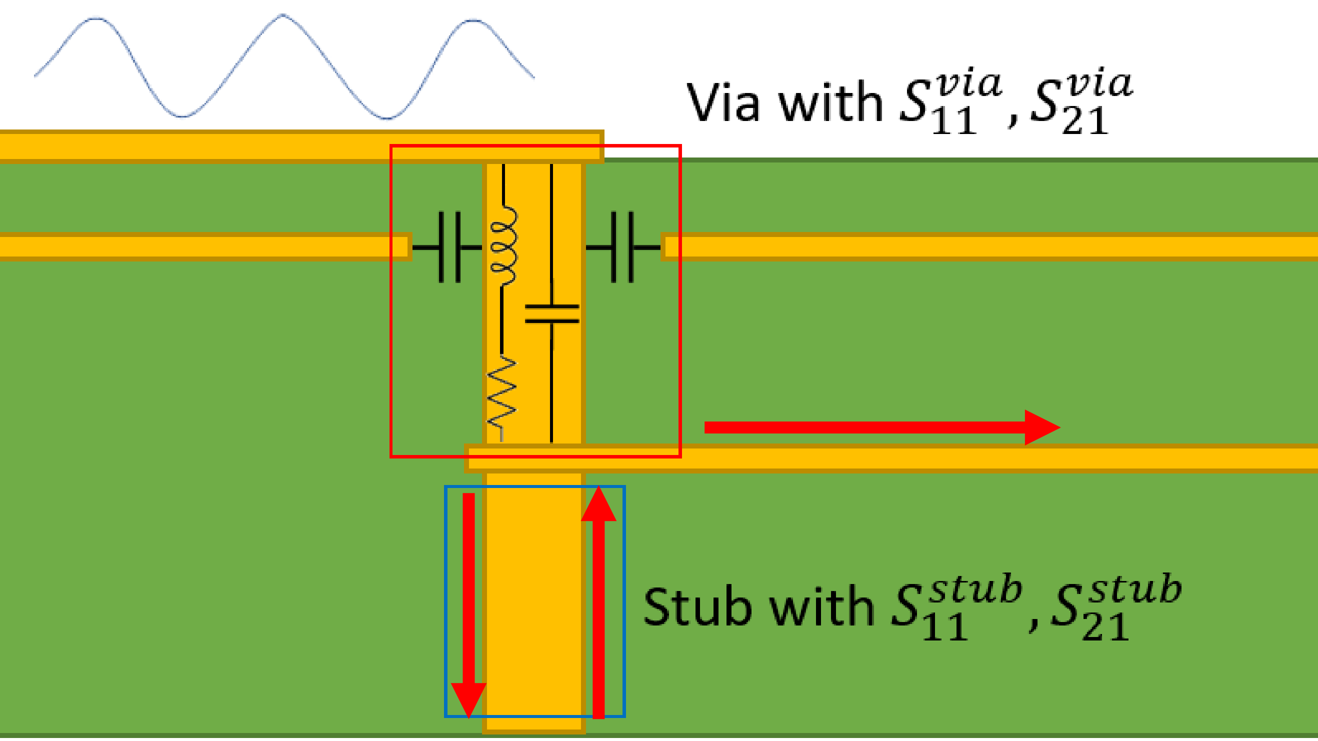
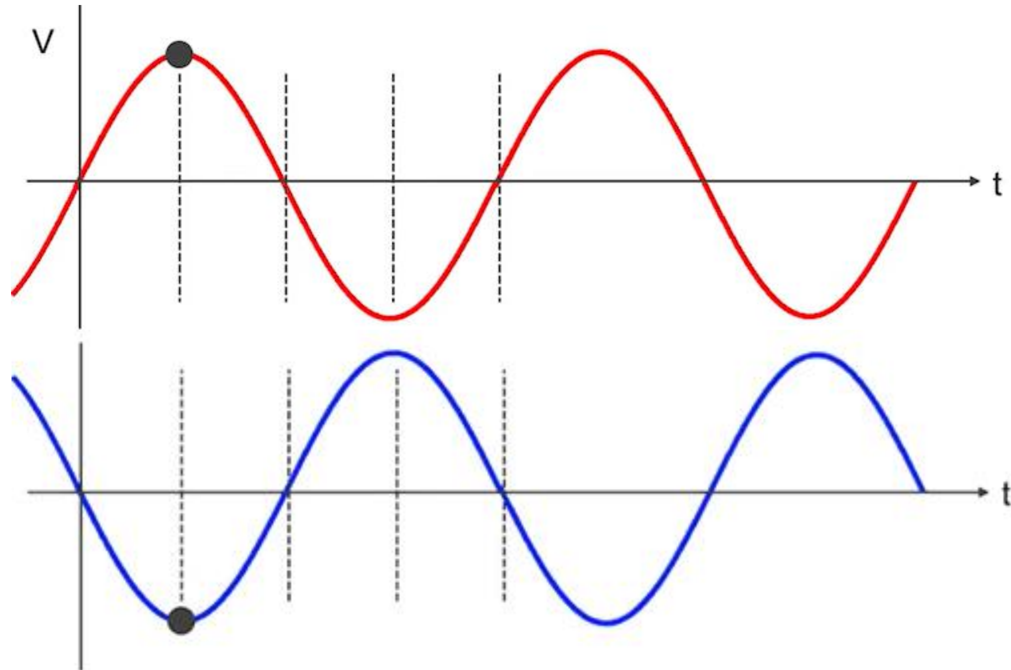


$$\Delta\varphi = 2\pi\left(\frac{L_{via} f \sqrt{Dk_{eff}}}{c}\right)$$

Signal destroyed whenever
$\Delta\varphi = 180^{\circ}$



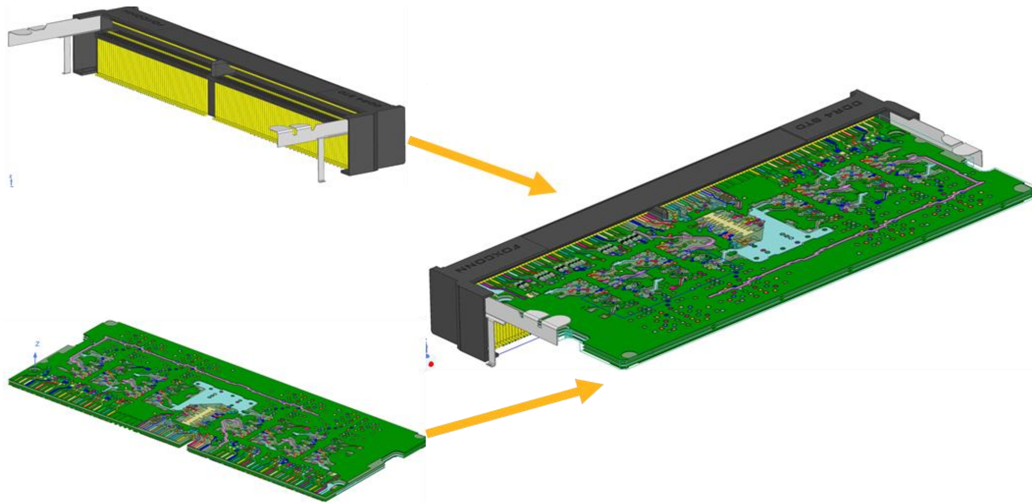
Low f $\quad Z_{via} \approx i\omega L + R_{DC} + \sqrt{\omega}(1+i)K(\omega)R_{skin}$

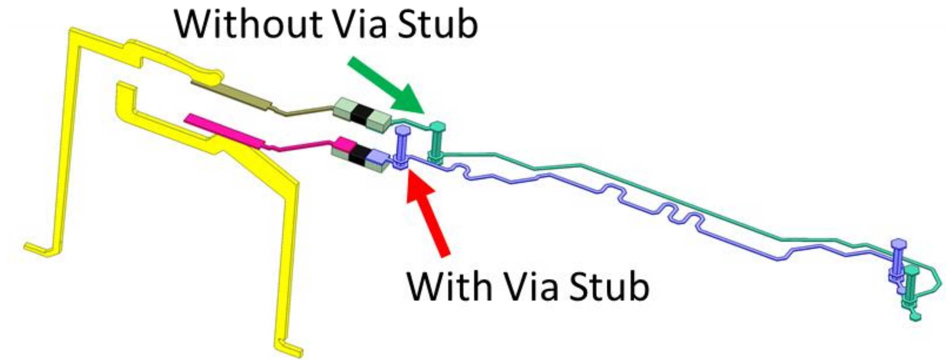
High f**:** Treat as a resonator (next slide), use input impedance

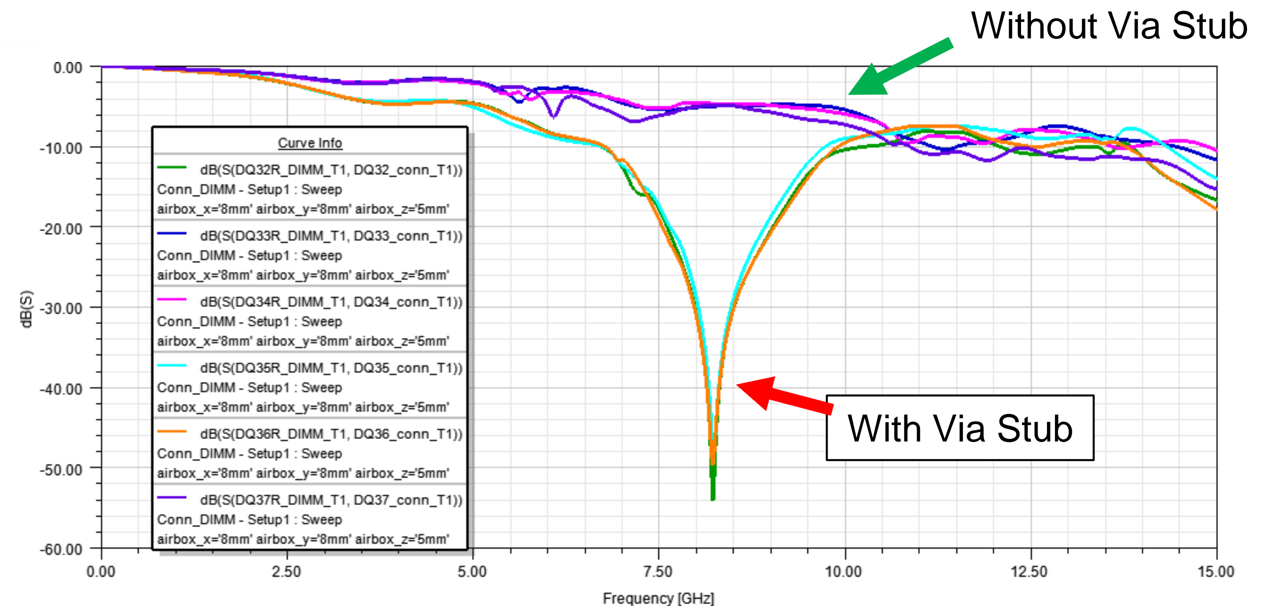
0.1 mm stub length: okay for signals up to roughly 150 GHz (typical FR4 substrate)

Via Stubs

- When should stubs be removed?







- Stubs act like transmission lines:

$$f_n = \frac{c_{vacuum}}{\lambda_n \sqrt{Dk_{eff}}}, \quad n = 1, 3, 5, \dots$$

Predicting Stub Loss Frequencies for Diff. Pairs

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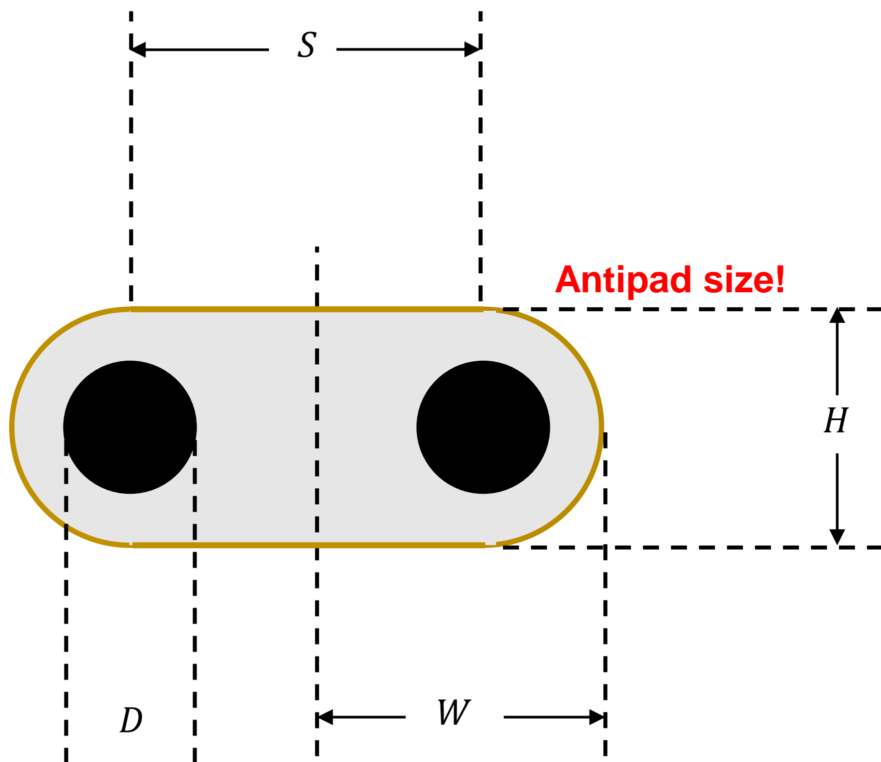
- Stubs create destructive interference at quarter wavelength resonances:

$$f_n = \frac{c_{vacuum}}{\lambda_n \sqrt{Dk_{eff}}} \qquad \lambda_n = \frac{4L}{n}, \quad n = 1, 3, 5, \ldots$$



$$Dk_{eff} = \left(\frac{Dk_{tr} + Dk_z}{2}\right) \frac{\ln\left(\frac{S}{D} + \sqrt{\left(\frac{S}{D}\right)^2 - 1}\right)}{\ln\left(\frac{W+H}{2D}\right)}$$

$$Dk_z \sim 1.2 Dk_{tr}$$

$$L_{max}[mils] \approx \frac{840}{GBaud * \sqrt{Dk_{eff}}}$$

Via delay: $$t_{Via} = \frac{L_{Via}\sqrt{Dk_{eff}}}{c_{vacuum}}$$

- Stubs create destructive interference at quarter wavelength resonances:

Preferred

Minimal stub equal to layer thickness

Not preferred

Long stub may limit bandwidth

Backdrilled

Leftover stub might be ***longer*** than the bottom layer thickness

Stay tuned for our Altium Designer demonstration.